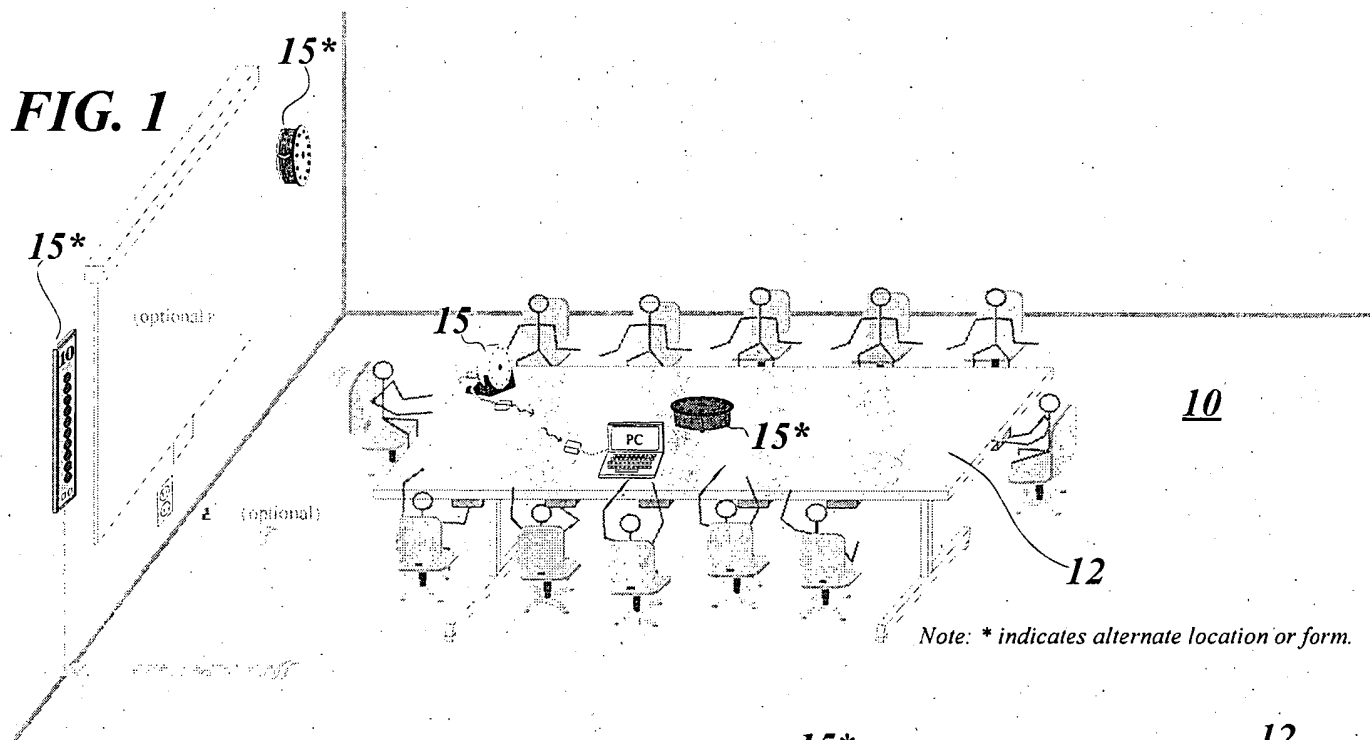
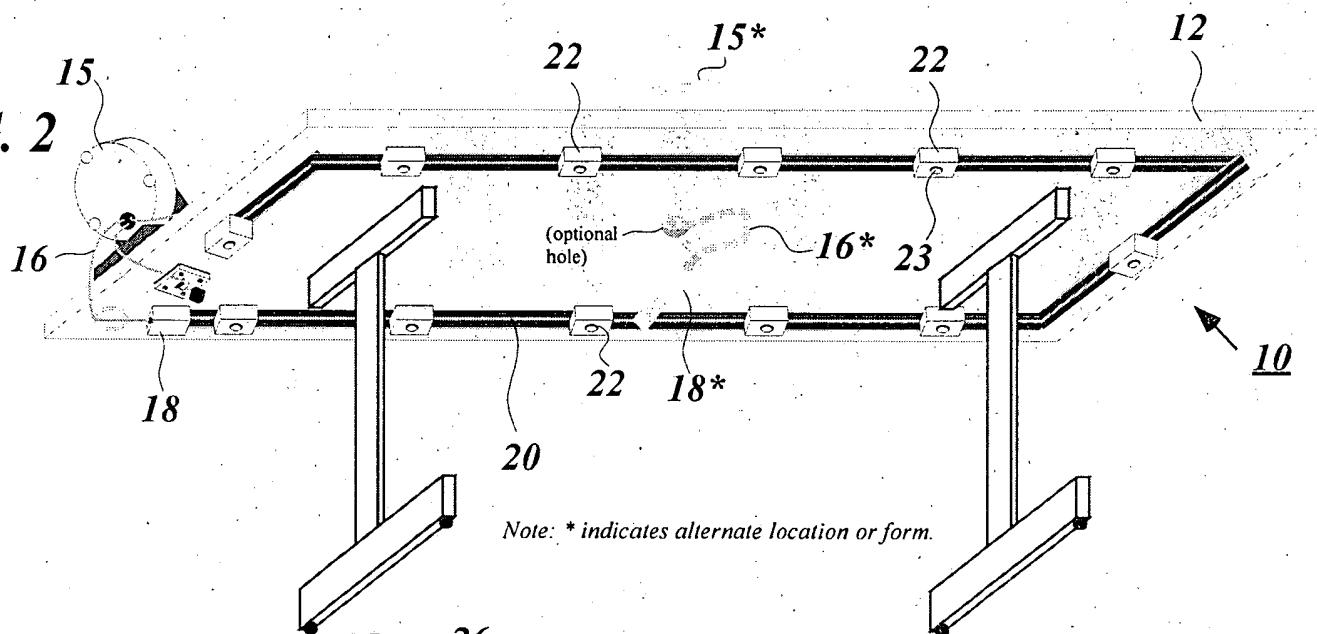


FIG. 1



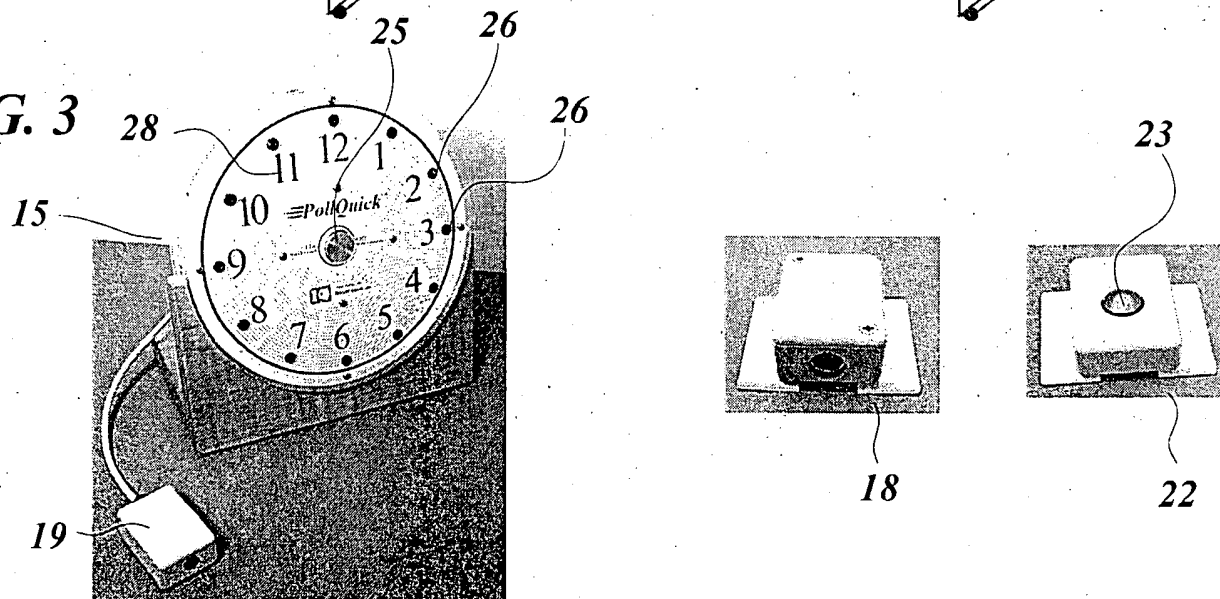
Note: * indicates alternate location or form.

FIG. 2



Note: * indicates alternate location or form.

FIG. 3





More Multiplexing can support 40 vote boxes, or more.
(e.g. 4 groups of 5 [times two] = 40 vote boxes)

The diagram illustrates a multiplexing system for 40 vote boxes, organized into four groups of five. The system uses two 5x5 switch matrices, labeled Group 0' and Group 0. The input lines are labeled Group 3 and Group 3', Group 2 and Group 2', Group 1 and Group 1', and Group 0 and Group 0'. The output lines are labeled c3, c2, c1, c0, and prime. The switch matrices are controlled by five lines labeled D05, D04, D03, D02, and D01. The output lines are also labeled f4, f3, f2, f1, and f0. The diagram shows how the switch matrices route the input lines to the output lines based on the control signals.

FIG. 4B

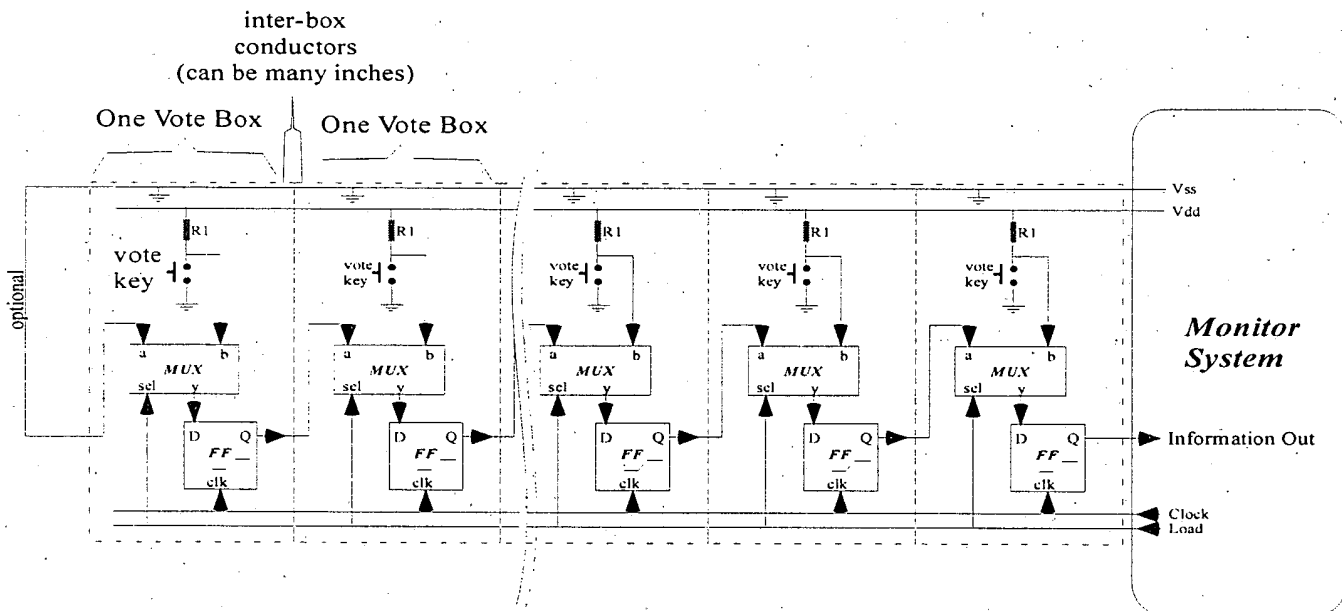
A Shift Register Version

Pros:

1. Can extend to large number of (identical) vote boxes.
2. All vote boxes are identical.
3. Data out (each Q) drives only small loads.

Cons:

1. Logic (ICs) required in each vote box.
2. Power (Vdd, Vss) must be supplied to the ICs.
3. More than 2 contacts per votebox are critical.
4. The clock drives multiple loads (unless made asynchronous).
5. Slow data out for given clock frequency (unless parallel paths used. See 3 below).
6. More FCC noise issues.
7. Press-on tool is more complicated (added cutting mechanism) since one or more conductors must be segmented.



Note: Simple refinements are possible:

1. We can supply Vdd (for FF & Mux) via the clock (rectified & LP filtered).
2. We can reduce the number of inter-box conductors by encoding "load" (for example) on other conductors. Even just 2 conductors can suffice.
3. More conductors can be used to simultaneously send several bits.
4. A 'counters with digital comparators' approach could replace the 'shift register' (above) approach.

FIG. 4C

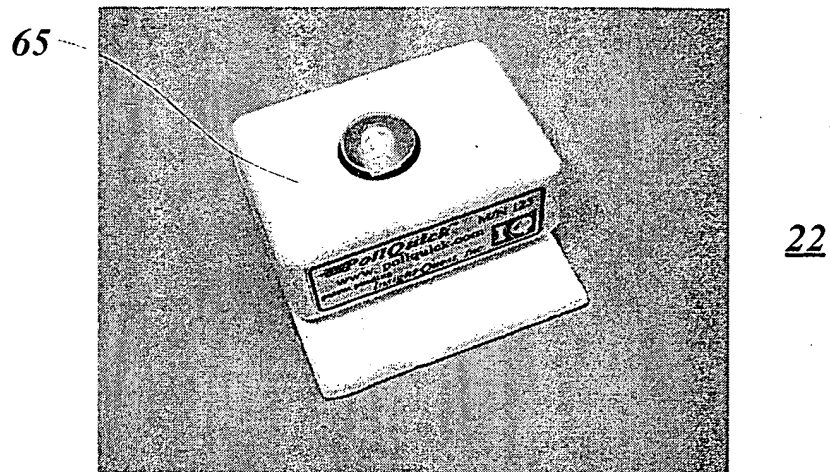


FIG. 5

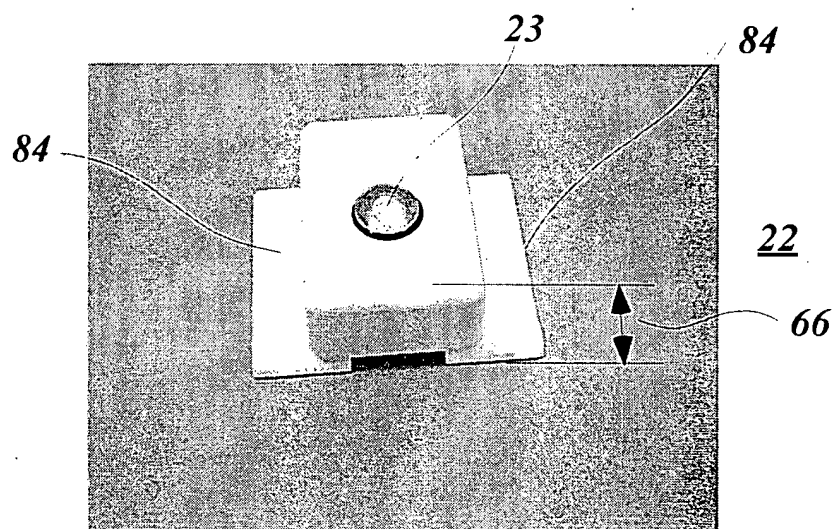


FIG. 6

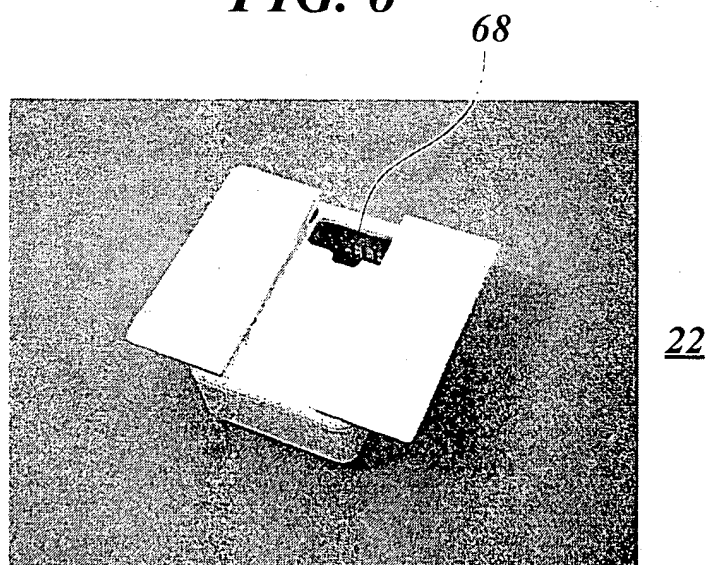


FIG. 7

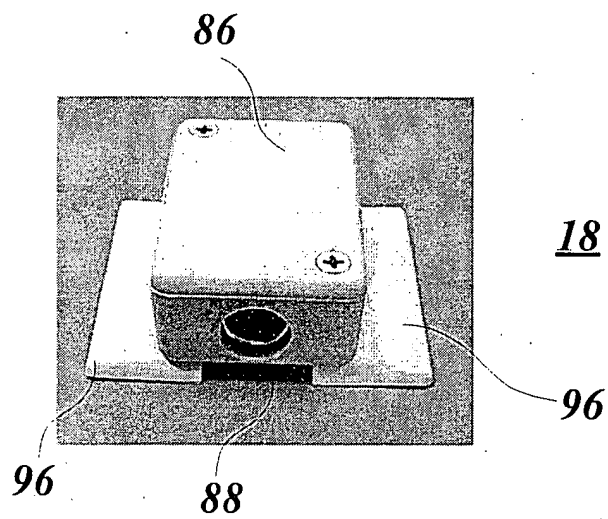


FIG. 8

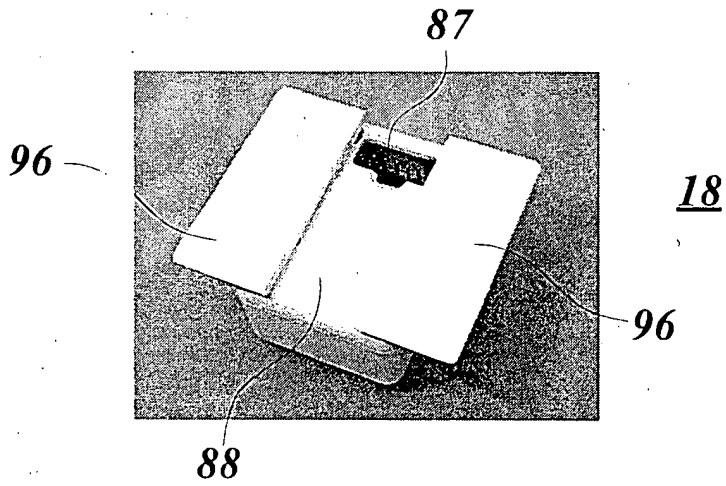


FIG. 9

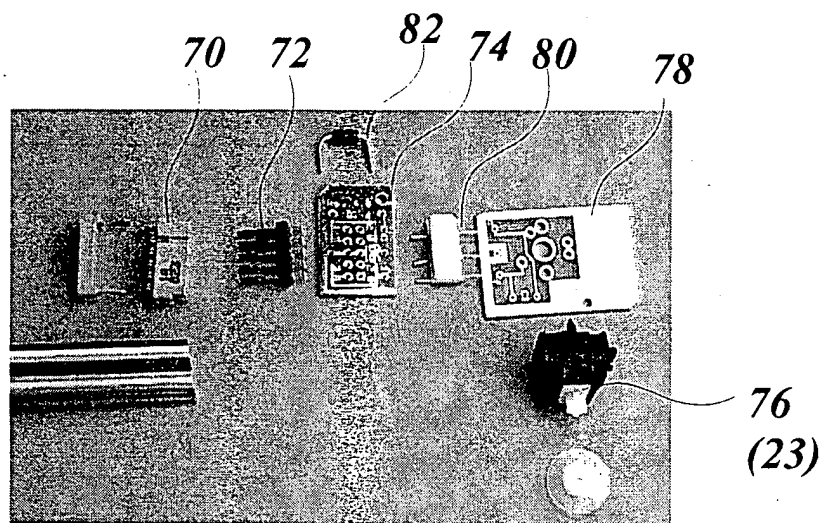


FIG. 10

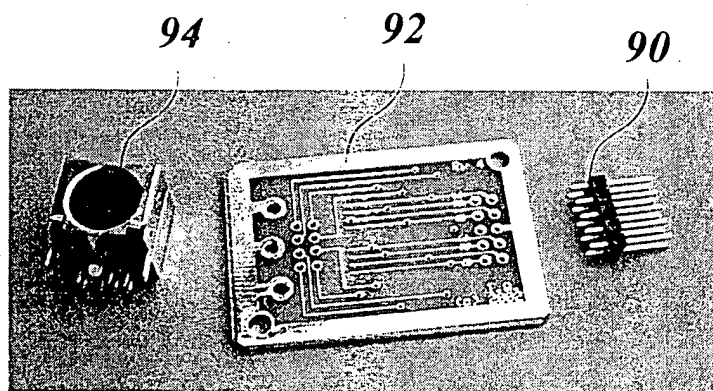


FIG. 11

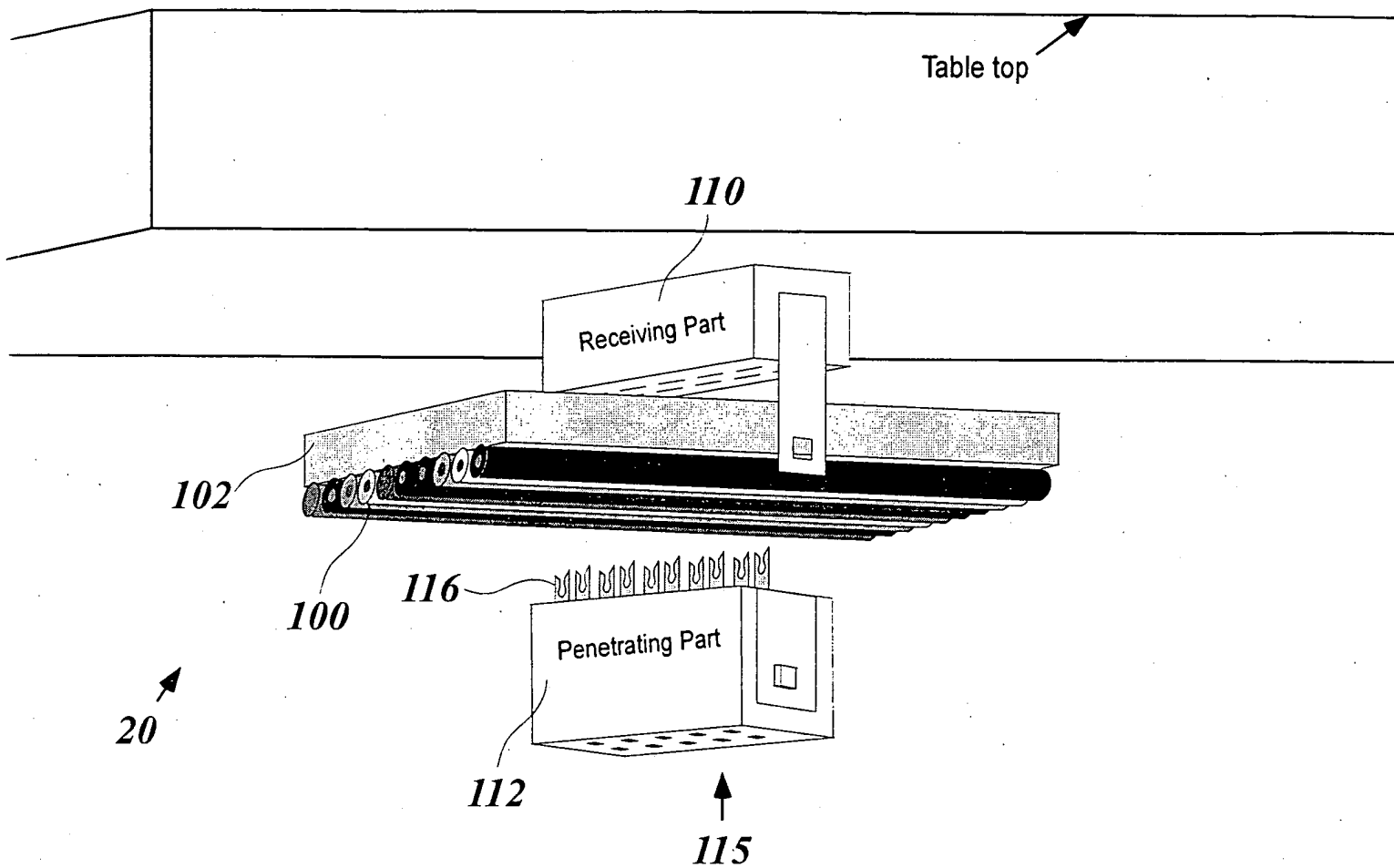


FIG. 12

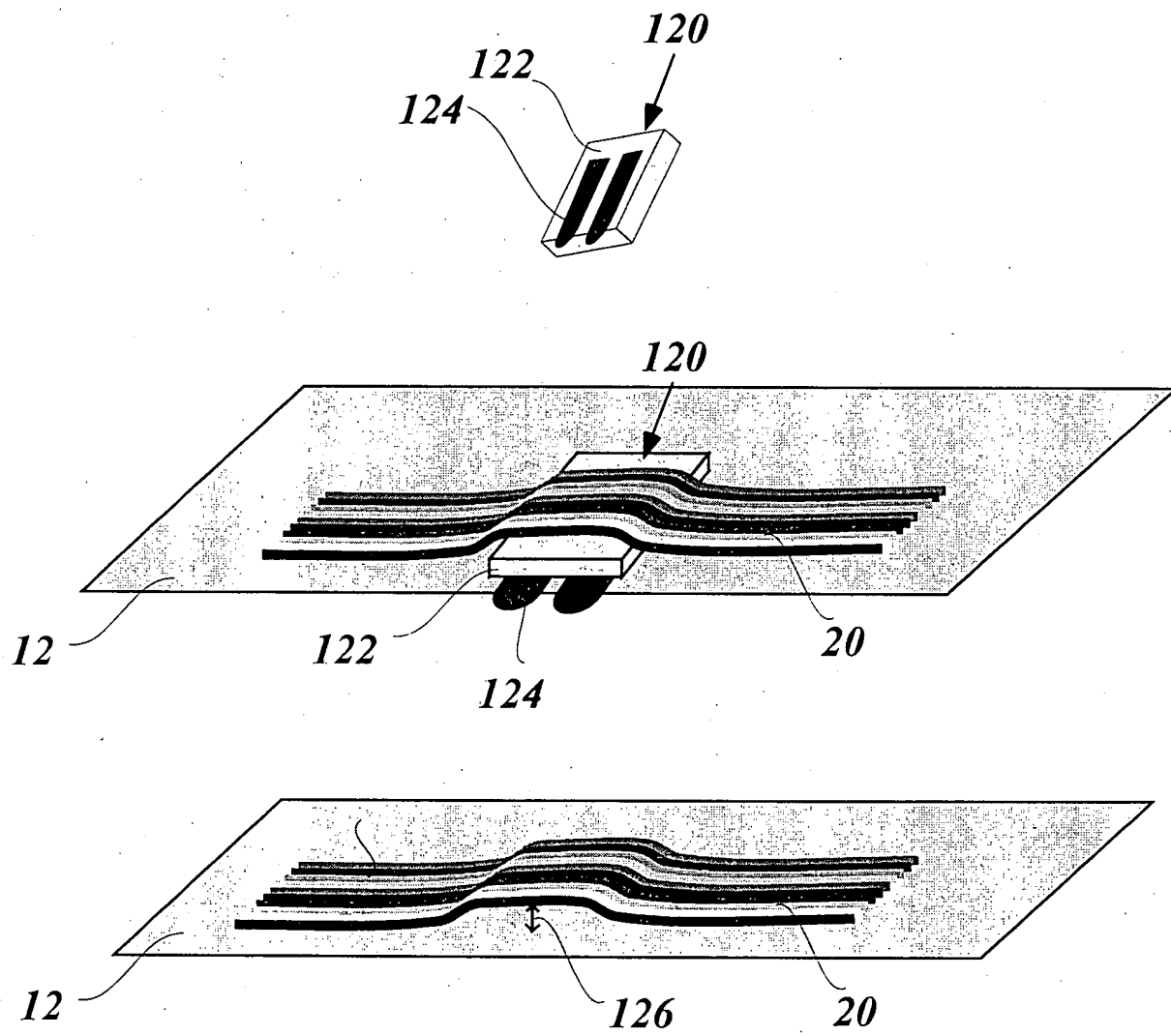


FIG. 13

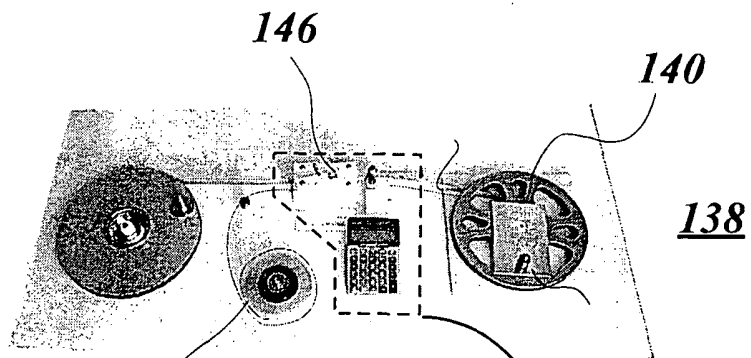


FIG. 14

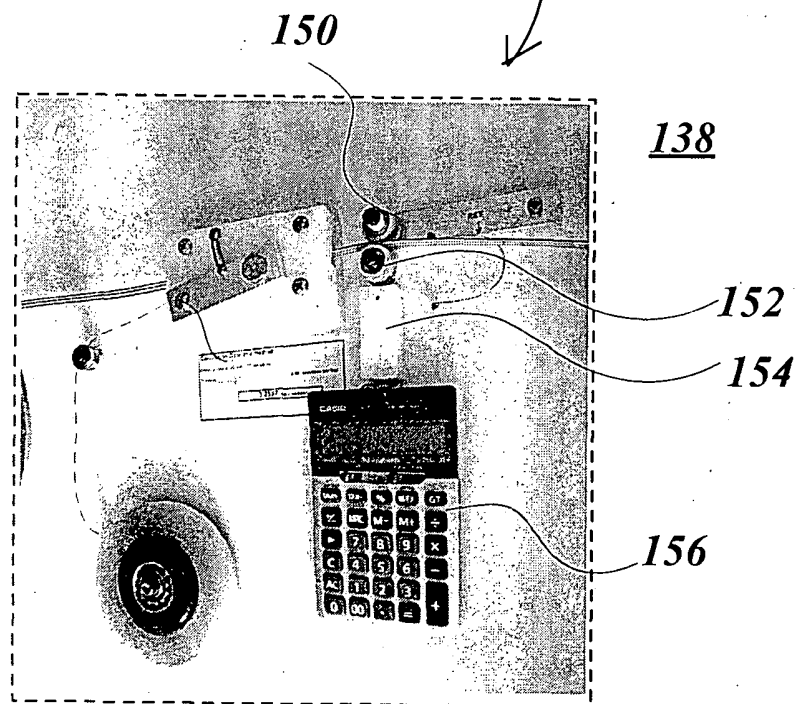


FIG. 15